

**AMENDMENTS TO THE CLAIMS:**

Please amend claims 2, 3, 4 and 6, as shown below.

This listing of claims will replace all prior versions and listings of claims in the  
Application:

**Claim 1 (original):** A memory module recovery method for use with a memory module which comprises a volatile memory and a non-volatile memory for recovering said volatile memory when determined as defective in an electric test, said method comprising the steps of:

previously storing a defective row address and a defective column address corresponding to a memory cell of said volatile memory determined as defective, and defective device information for discriminating said volatile memory determined as defective in said non-volatile memory;

transferring said defective row address, said defective column address and said defective device information stored in said non-volatile memory to said volatile memory upon start-up of a system which is equipped with said memory module;

holding said transferred defective row address, defective column address and defective device information in said volatile memory; and

accessing a redundant memory cell instead of said memory cell determined as defective when said memory module receives an address corresponding to said memory cell based on said defective row address, said defective column address and said defective device information held in said volatile memory.

**Claim 2 (currently amended):** ~~The memory module recovery method according to claim 1~~ A memory module recovery method for use with a memory module which comprises a

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volatile memory and a non-volatile memory for recovering said volatile memory when

determined as defective in an electric test, said method comprising the steps of:

previously storing a defective row address and a defective column address  
corresponding to a memory cell of said volatile memory determined as defective, and defective  
device information for discriminating said volatile memory determined as defective in said non-  
volatile memory;

transferring said defective row address, said defective column address and said  
defective device information stored in said non-volatile memory to said volatile memory upon  
start-up of a system which is equipped with said memory module;

holding said transferred defective row address, defective column address and  
defective device information in said volatile memory; and

accessing a redundant memory cell instead of said memory cell determined as  
defective when said memory module receives an address corresponding to said memory cell  
based on said defective row address, said defective column address and said defective device  
information held in said volatile memory,

wherein[[:]] said volatile memory comprises a plurality of fuse elements which  
can be blown out by laser light, said fuse elements being capable of holding information required  
to access said redundant memory cell instead of a memory cell determined as defective in a test  
at the end of a wafer manufacturing process.

**Claim 3 (currently amended):** A memory module comprising:

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~~a non-volatile memory for storing a defective row address and a defective column address corresponding to a memory cell in a volatile memory which is determined as defective in an electric test; and~~

a volatile memory for holding said a defective row address, said a defective column address and said a defective device information transferred thereto upon start-up of a system, said volatile memory including a redundant memory cell which is accessed instead of said a memory cell determined as defective in said volatile memory when said memory module receives an address signal corresponding to said memory cell determined as defective; and~~[[.]]~~

a non-volatile memory for storing ~~[[a]]~~ said defective row address and ~~[[a]]~~ said defective column address corresponding to ~~[[a]]~~ said memory cell in a volatile memory which is determined as defective in an electric test~~[[; and]]~~ .

**Claim 4 (currently amended):** ~~The memory module according to claim 3~~ A memory module comprising:

a volatile memory for holding a defective row address, a defective column address and a defective device information transferred thereto upon start-up of a system, said volatile memory including a redundant memory cell which is accessed instead of a memory cell determined as defective in said volatile memory when said memory module receives an address signal corresponding to said memory cell determined as defective; and

a non-volatile memory for storing said defective row address and said defective column address corresponding to said memory cell in a volatile memory which is determined as defective in an electric test,

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wherein[[:]] said volatile memory comprises a plurality of fuse elements which can be blown out by laser light, said fuse elements being capable of holding information required to access said redundant memory cell instead of a memory cell determined as defective in a test at the end of a wafer manufacturing process.

**Claim 5 (original):** A volatile memory having a redundant memory cell which is accessed instead of a defective memory cell in which a defect is found, said volatile memory comprising:

a defect information storage circuit for holding a defective row address and a defective column address transferred from the outside;

a device information storage circuit for determining whether or not said defective device information relates to said volatile memory itself to hold the result of the determination;

a row address comparator for comparing the defective row address stored in said defective information storage circuit with a row address supplied from the outside;

a column address comparator for comparing the defective column address stored in said defective information storage circuit with a column address supplied from the outside;

a redundant row decoder for activating a word line connected to said redundant memory cell when said defective row address matches said row address to enable an access to said redundant memory cell; and

a redundant column decoder for activating a bit line connected to said redundant memory cell when said defective column address matches said column address to enable an access to said redundant memory cell.

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**Claim 6 (currently amended):** ~~The volatile memory according to claim 5~~ A volatile memory having a redundant memory cell which is accessed instead of a defective memory cell in which a defect is found, said volatile memory comprising:

a defect information storage circuit for holding a defective row address and a defective column address transferred from the outside;

a device information storage circuit for determining whether or not said defective device information relates to said volatile memory itself to hold the result of the determination;

a row address comparator for comparing the defective row address stored in said defective information storage circuit with a row address supplied from the outside;

a column address comparator for comparing the defective column address stored in said defective information storage circuit with a column address supplied from the outside;

a redundant row decoder for activating a word line connected to said redundant memory cell when said defective row address matches said row address to enable an access to said redundant memory cell; and

a redundant column decoder for activating a bit line connected to said redundant memory cell when said defective column address matches said column address to enable an access to said redundant memory cell,

wherein[[:]] said redundant row decoder and said redundant column decoder each include a plurality of fuse elements which can be blown out by laser light for holding information required to access said redundant memory cell instead of a memory cell which is determined as defective in a test at the end of a wafer manufacturing process.

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